IN THE CLAIMS

Cancel claims 1-20 without prejudice to pursuit of the subject matter thereof in the future.

Claims 1-20 (canceled)

Claim 21 (new): An FET device comprising:

a substrate with a top substrate surface upon which a gate electrode stack is formed;

said gate electrode stack comprising a gate electrode formed over a gate dielectric layer, said gate dielectric layer being formed on said top substrate surface;

said gate electrode having a top gate electrode surface and having gate electrode sidewalls;

sidewall spacers formed on said gate electrode sidewalls aside from said gate electrode;

a cap layer having outer edges and a top formed on said top gate electrode surface;

notches formed in said outer edges of said cap layer recessed from said gate electrode sidewalls;

said notches in said outer edges of said cap layer being filled with protective plugs formed on said top of said gate electrode layer; and

said sidewall spacers reaching along said gate electrode sidewalls to above a level at which said protective plugs contact said gate electrode whereby said sidewall spacers are contiguous with and overlapping said protective plugs covering said sidewalls of said gate electrode.

Claim 22 (new): The FET device of claim 21 wherein a raised source region and a raised drain region are formed on said top substrate surface of said substrate aside from said spacers.

Claim 23 (new): The FET device of claim 21 wherein said protective plugs and said sidewall spacers are formed of dielectric, spacer material.

Claim 24 (new): The FET device of claim 22 wherein said protective plugs and said sidewall spacers are formed of dielectric, spacer material.

Claim 25 (new): The FET device of claim 21 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 26 (new): The FET device of claim 22 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 27 (new): The FET device of claim 23 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 28 (new): The FET device of claim 24 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 29 (new): The FET device of claim 21 wherein:

said gate electrode is composed of polysilicon; and

said cap layer comprises an ion implanted region formed in said polysilicon of said gate electrode.

Claim 30 (new): An FET device comprising:

a substrate with a top substrate surface upon which a gate electrode stack is formed;

said gate electrode stack comprising a gate electrode formed over a gate dielectric layer, said gate dielectric layer being formed on said top substrate surface;

said gate electrode being composed of polysilicon and having a top surface and having gate electrode sidewalls;

sidewall spacers formed on said gate electrode sidewalls aside from said gate electrode;

raised source/drain regions formed on said substrate surface aside from said sidewall spacers;

a cap layer having outer edges and a top formed in said top surface of said gate electrode comprising an ion implanted region formed in said polysilicon of said gate electrode;

notches formed in said outer edges of said cap layer recessed from said gate electrode sidewalls;

said notches in said outer edges of said cap layer being filled with protective plugs formed on said top of said gate electrode layer;

said sidewall spacers being contiguous with and overlapping said protective plugs covering said sidewalls of said gate electrode; and

said sidewall spacers reaching along said gate electrode sidewalls to above a level at which said protective plugs contact said gate electrode;

a raised source region and a raised drain region formed on said top substrate surface of said substrate aside from said spacers.

Claim 31 (new): The FET device of claim 30 wherein said cap layer comprises a thin amorphous silicon layer formed in said gate electrode composed of polysilicon which has been ion implanted with ions selected from the group consisting of germanium and silicon ions.

Claim 32 (new): The FET device of claim 30 wherein a raised source region and a raised drain region are formed on said top substrate surface of said substrate aside from said spacers.

Claim 33 (new): The FET device of claim 31 wherein said protective plugs and said sidewall spacers are formed of dielectric, spacer material

Claim 34 (new): The FET device of claim 32 wherein said protective plugs and said sidewall spacers are formed of dielectric, spacer material.

Claim 35 (new): The FET device of claim 30 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 36 (new): The FET device of claim 31 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 37 (new): The FET device of claim 32 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 38 (new): The FET device of claim 33 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

Claim 39 (new): The FET device of claim 34 wherein: said gate electrode is composed of polysilicon; and said cap layer comprises an ion implanted region formed in said polysilicon of said gate electrode.

Claim 40 (new): A SOI MOSFET device comprising:

a silicon layer has a surface with a gate electrode stack formed on said surface of said silicon layer;

said gate electrode stack comprises a gate dielectric layer formed on said surface of said silicon layer and a gate electrode with a top formed on said gate dielectric layer;

said gate electrode being composed of polysilicon and having sidewalls;

sidewall spacers formed on said sidewalls of said gate electrode;

a cap formed on top of said gate electrode, said cap having a periphery;

a hard mask formed on top of said cap;

said cap being undercut in said periphery of said cap in the form of a notch above said gate electrode and below said hard mask;

said notch being filled with dielectric plugs between said gate electrode and said cap to prevent exposure of said gate polysilicon of said gate electrode; and

said sidewall spacers reaching along said sidewalls of said gate electrode and overlapping said plugs; and

raised source/drain regions formed on said surface of said silicon layer aside from said spacers.